Claims

What is claimed is:

[c1] A method for modeling power of a pipelined processor, comprising:

breaking at least one design block of the processor into a plurality of sub-blocks;

determining a plurality of categories of power dissipation of each sub-block;

constructing a power simulation equation for each category of power dissipation of each sub-block;

determining coefficients of each power simulation equation;

applying a power simulation program to each power simulation equation to calculate the power of each sub-block; and

summing the power of each sub-block to calculate the power of the processor.

[c2] The method of claim 1, wherein the categories of power dissipation comprise:

a data dependent power category;

an architecture dependent power category; and

a constant power category.

[c3] The method of claim 2, wherein the data dependent power is dependent upon data values used and generated by a sub-block.

[c4] The method of claim 2, wherein the architecture dependent power is dependent on architectural activity within a sub-block.

[c5] The method of claim 2, further comprising:

approximating a performance range for the data dependent power category;

adding the approximated performance range for the data dependent power category to the constant power category.

[c6] The method of claim 2, further comprising:

approximating a performance range for the architecture dependent power category;

adding the approximated performance range for the architecture dependent power category to the constant power category.

[c7] The method of claim 1, wherein the coefficients of each power simulation equation comprise:

a minimum value;

a typical value; and

a maximum value.

[c8] A method for modeling the power of a pipelined processor, comprising:

a step of breaking the processor down into design sub-blocks;

a step of determining power simulation equations for each sub-block;

a step of running circuit simulations to generate coefficient values to be used in power equations;

a step of adding instructions to a cycle accurate simulator to extract activity data needed for equations;

a step of calculating results of the equations;

a step of running a benchmark program on the cycle accurate simulator;

a step of, during each cycle of a simulation run, calculating power for the sub-blocks; and

a step of developing metrics to summarize power over the run of the benchmark program.